REMARKS

Claims 37-39, 76-80, and 82-99 are currently pending in the present patent application, with claims 36 and 81 having been cancelled. In an Office Action mailed July 3, 2002, the Examiner rejected claims 36, 39, 81, and 85 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,376,593 to Sandhu *et al.* ("Sandhu") and rejected claims 81, 83, and 85 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,201,276 B1 to Agarwal *et al.* ("Agarwal"). The Examiner allowed claims 76-80 and 86-99, and indicated claims 37, 38, 82, and 84 would be allowable if rewritten in independent form.

Claims 37 and 82 have been rewritten in independent form and are thus now in condition for allowance. These amendments do not narrow the scope of these claims, but instead merely rewrite the claims in independent form. Claims 37 and 82 are thus in condition for allowance, and claims 38-39 and 83-85, which depend from these independent claims, are similarly in condition for allowance.

Neither the Sandhu nor the Agarwal references discloses or suggests incorporating an oxygen-free material directly into the surface of a first conductive layer and thereafter forming a second conductive layer thereon, nor does either reference disclose or suggest exposing a conductive layer to a material selected from the recited group as set forth in several of the claims. Accordingly, the combinations of elements recited in all pending claims are allowable.

All pending claims are now in condition for allowance, and favorable consideration and a Notice of Allowance are respectfully requested. The Examiner is requested to contact the undersigned at the number listed below for a telephone interview if, upon consideration of this amendment, the Examiner determines any pending claims are not in condition for allowance. The undersigned also requests the Examiner to direct all future correspondence to the address set forth below in the event the Examiner shows a different correspondence address for the attorney of record.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with Markings to Show Changes Made**".

Respectfully submitted,

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Enclosures:
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

Paragraph beginning at line 4 of page 8 has been amended as follows:

Still other gases include diborane (B_2H_6); phosphine (PH_3); and carbon-silicon compounds such as methylsilane (CH_3SiH_3) and hexamethyldisilane $(CH_3)_3Si\text{-}Si(CH_3)_3$; and hexamethyldisilazane (HMDS). Additional alternate embodiments of the current invention use hydrazine (N_2H_4), monomethylhydrazine, carbon tetrafluoride (CF_4), CHF_3, HCl, and boron trichloride (BCl_3), which are also useful in passivating dielectrics, as addressed in copending application 09/114,847, now issued as U.S. Patent No. 6,201,276 B1. Also included are mixtures of any of the gases or types of gases described above. Exemplary non-plasma process parameters using these other gases include a flow rate of about 2 sccm to about 400 sccm for these gases; a flow rate of about 50 sccm to about 100 sccm for an inert carrier gas such as He or Ar; a temperature ranging from about 150 to about 600 degrees Celsius, a pressure ranging from about 50 millitorr to about 1 atmosphere (760 torr); and a process time ranging from about 50 to about 500 seconds. Again, one skilled in the art is aware that these parameters can be altered to achieve the same or a similar process.

In the Claims:

Claims 36 and 81 have been cancelled.

Claims 37, 38, 39, 82, 84, and 85 have been amended as follows:

37. (Amended) A method of forming a semiconductor device, comprising:

depositing a first conductive layer having a surface and having an ability to associate with oxygen;

incorporating an oxygen-free material directly into said surface to passivate the surface of said first conductive layer to reduce the ability of the first conductive layer to associate with oxygen;

depositing a second conductive layer on said surface after incorporating the oxygen-free material into the surface;

exposing said second conductive layer to a thermal process; [The method in claim 36,] and wherein[:] said step of depositing a first conductive layer comprises depositing a capacitor plate;

and wherein said method further comprises depositing an insulator over said second conductive layer; and

said step of exposing said second conductive layer to a thermal process comprises flowing said insulator.

38. (Amended) The method in claim [36] 37, wherein:

said step of depositing a first conductive layer comprises depositing a plug; and

said step of exposing said second conductive layer to a thermal process comprises

flowing said second conductive layer.

39. (Amended) The method in claim [36] 37, wherein said step of exposing said second conductive layer to a thermal process comprises exposing said second conductive layer to an alloy process.

82. (Amended) A method of forming a semiconductor device, comprising

providing a first conductive layer having a surface and having an ability to associate with oxygen;

placing the surface of the first conductive layer in direct contact with an oxygen-free atmosphere under appropriate conditions to passivate the surface and reduce the ability of the first conductive layer to associate with oxygen;

providing a second conductive layer on the surface of the first conductive layer;

subjecting the second conductive layer to a thermal process; and [The method in claim 81] wherein depositing a first conductive layer forms a capacitor plate and

wherein the process further comprises depositing an insulator over the second conductive layer and wherein exposing the second conductive layer to a thermal process comprises flowing the insulator.

84. (Amended) The method in claim 82 [81] further comprising depositing a plug on which the first conductive layer is thereafter deposited, and wherein exposing the second conductive layer to a thermal process comprises flowing the second conductive layer.

85. (Amended) The method in claim 82 [81], wherein exposing the conductive layer to a thermal process comprises exposing the conductive layer to an alloy process.